first output signal after the first output signal is changed by a predetermined amount by the first drive circuit.

26. (New) The output buffer circuit according to claim 25, wherein the first drive circuit receives an input signal having a sharp waveform and generates the first output signal that has a gentle waveform.

27. (New) The output buffer circuit according to claim 25, further comprising a delay circuit, connected to the output terminal, for delaying the first output signal and generating a delayed output signal.

REMARKS

The above amendments and the following remarks are fully and completely responsive to the Office Action dated April 30, 2002. Claims 1-27 are pending in this application with claims 19-27 added and claims 12-18 cancelled by the present amendment. No new matter has been entered. Claims 1-11 and 19-27 are presented for consideration.

In the outstanding Office Action, claims 1-11 were rejected under 35 USC §102(e) as being anticipated by Wert (U.S. Patent No. 6,281,706). In making this rejection, the Office Action asserts that Wert teaches each and every element of the claimed invention. Applicants request reconsideration and withdrawal of this rejection.

Claim 1 recites a method of controlling an output buffer circuit for generating an output signal and outputting the output signal from an output terminal. The buffer circuit includes a first drive circuit for receiving an input signal and a second drive circuit

connected to the output terminal. The second drive circuit has a lower output impedance than the first drive circuit. The method includes generating a first output signal having a first state in accordance with the input signal using the first drive circuit. The second drive circuit is driven to generate a second output signal having the first state after the first output signal is changed by a predetermined amount by the first drive circuit.

Accordingly, the present invention, as set forth in claims 1 and 2, is directed to a method for controlling an output buffer circuit including a first drive circuit and a second drive circuit. The method includes driving the second drive circuit after a first output signal of the first drive circuit is changed by a predetermined amount.

The present invention, as set forth in claim 5, is also directed to an output buffer circuit. This circuit includes a first drive circuit connected to an output terminal, for receiving an input signal and generating a first output signal having a first state. A second drive circuit is connected to the output terminal and has a lower impedance than the first drive circuit. The second drive circuit generates a second output signal having the first state. A control circuit is connected to the second drive circuit and generates a first control signal for driving the second drive circuit on the basis of the input signal and the first output signal after the first output signal of the buffer circuit is changed by a predetermined amount by the first drive circuit.

Consequently, after the signal output by the first drive circuit changes by the predetermined amount, the second drive circuit having a low output impedance

characteristic is driven so that the low output impedance characteristic is provided in the static state of the output signal.

Wert is directed to a boost circuit including a first drive circuit (701, 711) a second drive circuit (705, 717), and two inventors (707, 709). The second drive circuit of Wert is automatically driven when the delay time of the two inventors (707, 709) has passed after the transistor (701) of the first drive circuit is turned on.

When transitioning from a logic low to a logic high, Wert teaches that because of propagation delay, transistor 705 is turned on after transistor 701. Because of the relative threshold voltages, transistor 705 is turned off before transistor 701. Wert also teaches that during a logic high to a logic low transition, transistor 717 is turned on after transistor 711 and then turned off before transistor 711 is turned off. Consequently, the second drive circuit (705, 717) of Wert is only driven while the first drive circuit (701, 711) is driven.

In contrast, the present invention, as set forth in claims 1, 2 and 5, recites driving the second drive after the first output signal of the first drive circuit is changed by a predetermined amount. Thus, the second drive circuit is not driven when the output signal of the first drive circuit is below the predetermined amount even if the first drive circuit has been driven. Wert does not and cannot teach driving the second drive circuit after the output signal of the first drive circuit changes by a predetermined amount because the second drive circuit is automatically driven while the first drive circuit is driven. Accordingly, the present invention is neither disclosed nor suggested by Wert. Furthermore, due to the differences between the present invention and Wert, Wert is

unable to provide the advantages of the present invention. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-2 and 5 under 35 USC §102(b).

Claims 3-4 and 6-11 depend either directly or indirectly from claims 2 and 5 respectively. Therefore, it is respectfully submitted that these claims are not anticipated by or obvious in view of Wert for at least the reasons set forth with regard to claims 1, 2 and 5 above.

New claims 19-27 have been added to claim additional features of the present invention. These claims are patentable for at least the reasons discussed above.

Applicants amendments and remarks clearly overcome the rejections set forth in the Office Action dated April 30, 2002. Specifically, applicants remarks have distinguished claims 1-11 and 19-27 from Wert, and thus have overcome the rejection of these claims under 35 USC §102(e). Consequently, claims 1-11 and 19-27 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-11 and 19-27.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned Attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to Attorney Docket No. 108075-00022.

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS
AS REQUIRED UNDER 37 CFR §1.121

1. (Once Amended) A method of controlling an output buffer circuit [comprising] for generating an output signal and outputting the output signal from an output terminal, wherein the output buffer circuit includes a first drive circuit for receiving an input signal [having a sharp waveform and generating an output signal that has a gentle waveform and is output from an output terminal of the output buffer circuit], and a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, the method comprising the steps of:

[changing the] generating a first output signal having a first state in accordance with [a change in] the input signal using the first drive circuit; and

driving the second drive circuit to generate a second output signal having the first state after the first output signal is changed by a predetermined amount by the first drive circuit.

2. (Twice Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, [wherein the first and second output transistors generate an output signal having gentle waveform in response to an input signal having a sharp waveform,] the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a fourth output transistor

connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating [the] a first output signal having a first state in accordance with the input signal using the first drive circuit;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit to generate a second output signal having the first state [in accordance with the control signal] after the first output signal is changed by a predetermined amount by the first drive circuit.

3. (Once Amended) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal by turning on the first output transistor;

the driving step includes turning on the third output transistor with the control signal; and

the method further comprises step of substantially simultaneously turning off the first and third output transistors in accordance with a change in the input signal.

4. (Once Amended) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal by turning on the second output transistor;

the driving step includes turning on the fourth output transistor with the control signal; and

the method further comprises a step of substantially simultaneously turning off the second and fourth output transistors in accordance with a change in the input signal.

5. (Twice Amended) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal [having a sharp waveform] and generating [an] a first output signal [that has a gentle waveform and is output from an output terminal of the output buffer circuit] having a first state;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, wherein the second drive circuit generates a second output signal having the first state;

[a delay circuit, connected to the output terminal, for delaying the output signal and generating a delayed output signal;] and

a first control circuit, connected [between the delay circuit and] to the second drive circuit, for [receiving the input signal and the delayed output signal and] generating a first control signal for driving the second drive circuit on the basis of the input signal and the first output signal after the first output signal is changed by a predetermined amount by the first drive circuit.

6. (Once Amended) The output buffer circuit according to claim 5, wherein the first drive circuit includes a first output transistor connected between a first power supply and the output terminal and a second output transistor connected between a

second power supply and the output terminal, wherein the first and second output transistors generate the first output signal [having the gentle waveform]; and

the second drive circuit includes a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors.

7. (Once Amended) The output buffer circuit according to claim 6, wherein the first control circuit turns on the third output transistor with the first control signal [in response to the delayed output signal] after the first output transistor is turned on by the input signal, and the first control circuit turns on the fourth output transistor with the first control signal [in response to the delayed output signal] after the second output transistor is turned on by the input signal.

11. (Once Amended) The output buffer circuit according to claim 10, wherein the first control circuit supplies the first control signal to each of the sub-drive circuits based on the input signal[, the delay signal] and a select signal.